THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YOSHIMITSU INAMORI
and KOICHI ODA

Appeal No. 1998-3064
Application No. 08/445,867[1]

HEARD: October 21, 1999

Before JERRY SMITH, FLEMING, and BARRY, Administrative Patent Judges.

BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection of claims 2 and 4-12. We reverse.

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[1] The application was filed on May 22, 1995. It is a divisional of Application Serial No. 08/191,723, which was filed on February 4, 1994. The latter application was a continuation of Application Serial No. 07/743,608, which was filed on August 9, 1991 and is now abandoned.

BACKGROUND

The invention at issue in this appeal relates to a liquid crystal display (LCD). Specifically, the invention is circuitry for reading data from and writing data to the addressable display space of the LCD. The circuitry includes a common drive circuit and a plurality of segment-drive circuits. Under control of a central processing unit (CPU), the circuitry reads data from and writes data to addressable positions of the display space in a row-direction or a column-direction or both. Such circuitry is particularly useful for LCDS having long rows.

Claim 7, which is representative for our purposes, follows:

> 7. A display control circuit for a display unit having a plurality of addressable positions arranged in a matrix, comprising:
>
> a plurality of segment drive circuits connected to the display unit in a line writing/reading direction, each said segment drive circuit being provided for the writing/reading of data to/from only a predetermined addressing range of addressable positions of a total range of addressable positions of the matrix, said predetermined addressing range of addressable positions being in the line

writing/reading direction and in an orthogonal direction, each said segment drive circuit producing a relative address within the predetermined addressing range associated with the segment drive circuit in response to address data and a selection signal input thereto for writing/reading data input thereto at/from the generated relative address;

a common drive circuit responsive to input data for driving a common electrode of the display unit and

for selecting one of the segment drive circuits and providing address data for writing/reading data to/from said relative address and for providing/receiving display data only to/from the selected segment drive circuit; and

a processing unit connected to the common drive unit for providing said input data including display data and address data and for receiving output data read from the display unit.

The references relied on in rejecting the claims follow:

Mano et al.	4,985,698	Jan. 15, 1991
Koyama (UK Patent Application)	2,224,873	May 16, 1990.

Claims 2 and 4-12 stand rejected under 35 U.S.C. § 103(a) as obvious over Koyama in view of Mano. Rather than repeat the arguments of the appellants or examiner in toto, we refer the reader to the briefs and answer for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejection and evidence advanced by the examiner. Furthermore, we duly considered the

arguments of the appellants and examiner. After considering the totality of the record, we are persuaded that the examiner erred in rejecting claims 2 and 4-12. Accordingly, we reverse.

We begin by noting three principles from In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). (1) In rejecting claims under § 103, the patent examiner bears the initial burden of establishing a prima facie case of obviousness. (2) A prima facie case is established when teachings from the prior art would appear to have suggested the claimed subject matter to a person of ordinary skill in the art. (3) If the examiner fails to establish a prima facie case, an obviousness rejection will be reversed. With these in mind, we analyze the appellants' arguments.

Regarding claims 2 and 4-12, the appellants make several related arguments. They argue, "neither reference provides addresses to the segment drive circuits identified by the Examiner ...." (Appeal Br. at 8.) The appellants add the following argument.

> Koyama, for example, clearly indicates that elements 11 through 13 are not operative to output address and associated display data, as claimed, but merely receive data to be displayed wherein the display data is [sic, are] produced by either the character generator 4 or the graphic data produced by control circuit 5. (Id. at 9.)

They further argue, "Similar observations and conclusions are made with regard to the teachings of Mano wherein shift register elements 9 and 10 merely provide display data to the left and right halves of the display device 11 ...." (Id. at 11.)

The examiner replies, "Koyama clearly teaches the CPU 1 for outputting the address data to the column drive circuits .... Moreover, the feature providing addresses to the segment drive circuit is well-known in the art, even acknowledged by Appellant; see page 6, lines 4-9 of the specification." (Examiner's Answer at 7-8.) He adds, "Mano clearly teaches a plurality of segment driver circuits (9 and 10). The segment driver circuit (9) is used to control display dat [sic, data] in a left hand panel and the segment driver circuit (10) is used to control display data in a right hand panel. The

predetermined addressing range is determined by drive circuits (9 and 10)." (Id. at 11.)

The appellants respond, "There is no teaching or suggestion in the applied references of programming, much less of how to program, the CPU to provide the address information as claimed. Moreover, using a programmed CPU to provide addresses to the display device is contrary to the specific teachings of the instant application." (Reply Br. at 2.) We agree with the appellants.

Independent claim 2 specifies in pertinent part the following limitations:

> a plurality of row drive means connected to a display means having a display space ..., each said row drive means being provided for only a predetermined addressing range of a total range of addresses within the display space and each being operative to output relative row address data within the predetermined addressing range and display data respectively associated therewith, and
>
> column drive means ... for outputting column address data to the display means ... and for outputting relative row and column address data and display data for each selected row drive means, and
>
> control means for outputting display data and address data to the column drive means ....

Similarly, independent claim 4 specifies in pertinent part the following limitations:

> a plurality of address output means connected to a display means having a display space ... each of said plurality being operative to output relative address data for only a predetermined address range portion of a total range of addresses in said display means and for outputting/receiving display data to/from the display means,
> other address output means ... for outputting said relative address data ... and for outputting address data which is relative to the predetermined address range of the selected one of the plurality of address output means, and
> control means for outputting to the other address output means ... address data and display data for writing/reading in the display space.

Also similarly, independent claim 7 specifies in pertinent part the following limitations:

> A display control circuit for a display unit having a plurality of addressable positions arranged in a matrix, comprising:
> a plurality of segment drive circuits connected to the display unit ... each said segment drive circuit being provided for the writing/reading of data to/from only a predetermined addressing range of addressable positions of a total range of addressable positions of the matrix ... each said segment drive circuit producing a relative address within the predetermined addressing range associated with the segment drive circuit in response to address data and a selection signal input thereto for writing/reading data input thereto at/from the generated relative address;

> a common drive circuit responsive to input data for driving a common electrode of the display unit ... and providing address data for writing/reading data to/from said relative address and for providing/receiving display data only to/from the selected segment drive circuit; and
>
> a processing unit connected to the common drive unit for providing said input data including display data and address data ....

Giving claims 2, 4, and 7, their broadest reasonable interpretation, the claims recite a processor providing address data and display data to a common drive circuit; the common drive circuit responsively providing the address data and display data to a selected segment drive circuit; and the selected segment drive circuit responsively generating a relative address for the display data.

The examiner fails to show a teaching or suggestion of these limitations in the prior art. Koyama teaches a CPU 1 that designates address data for reading display data from and writing data to a RAM 2. P. 8, ll. 15-24. The reference also teaches a common drive circuit 14 that drives horizontal common electrodes of an LCD 3 and a segment driving circuit 13 that drives vertical segment electrodes of the LCD. P. 12, ll. 9-16. Koyama, however, does not teach providing address data and display data to the common drive circuit, the common drive circuit providing the address data and display data to the segment drive circuit; or the segment drive circuit generating a relative address for the display data.

Mano does not cure these deficiencies. The reference merely teaches a Y drive circuit YDV 12 for scanning an LCD 11 in a vertical direction, col. 5, ll. 40-49, and for providing display data to a left-hand X drive circuit XDVL 9 and a right-hand X drive circuit XDVR 10 for controlling display on the LCD 11. Col. 4, l. 57 - col. 5, l. 5. Mano, however, does not teach providing address data and display data to the Y drive circuit, the Y drive circuit providing the address data and display data to the X drive circuits, or the X drive circuits generating a relative address for the display data. Consequently, the references neither teach nor would have suggested a processor providing address data and display data to a common drive circuit; the common drive circuit responsively providing the address data and display data to a selected segment drive circuit; and the selected segment drive circuit responsively generating a relative address for the display data as claimed.

For the foregoing reasons, the examiner has not established a prima facie case of obviousness. Therefore, we reverse the rejection of claims 2 and 4-12.

CONCLUSION

To summarize, the examiner's rejection of claims 2 and 4-12 under 35 U.S.C. § 103(a) is reversed.

REVERSED

JERRY SMITH Administrative Patent Judge	)
MICHAEL R. FLEMING Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)

LLB/dal

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